REMARKS

Reconsideration and allowance of this patent application are respectfully requested.

Applicants acknowledge with appreciation the indication that claims 6 and 7 contain allowable subject matter.

As requested, the title of the invention is changed to be even more clearly indicative of the invention to which the claims are directed; the specification is amended to correct minor informalities found during preparation of this response; and Figures 11-17 are designated with the legend --PRIOR ART--.

Claims 9 and 13-19 are amended to overcome the Section 101 and Section 112 issues identified in the office action. As such, withdrawal of the rejections of these claims on these bases is respectfully requested.

Claims 1, 3-5, 9, 13 and 14 were rejected under 35 U.S.C. Section 103(a) as allegedly being unpatentable over JP 63-117445. As explained in the present specification, JP 63-117445 discloses a process in which a bump is formed on each IC of a semiconductor wafer prior to polishing. Next, grooves are formed by a dicing process. The front face of the semiconductor wafer is then coated with wax having chemical etching resistance and the wafer is then immersed in a chemical etchant so that the rear face of the wafer is etched to have a predetermined thickness. Then, the semiconductor wafer is washed by water to remove the etchant and the wax is removed by a solvent. Thereafter, the wafer is subjected to a breaking process to separate it into semiconductor chips.

However, in JP 63-117445, wax gets into the grooves between the chips, thereby coating the cut faces with wax. In particular, Figure 2(d) of JP 63-117445 illustrates that the wax gets into the grooves between the chips and Figure 2(f) shows adjacent chips adhered together by the wax in a post-etching state. When wax gets into the grooves between the chips, the sides of the chips damaged by dicing cannot be etched by etchant, even if the etching process removes the residual portions. In contrast, the method of claim 1 calls for, among other things, the chemical etching to remove damaged areas in a cut face of the semiconductor wafer resulting from the semi-full dicing process.

And while JP 63-117445 describes that "a smooth cut face is obtained without cracks and protrusions due to cleavage of monocrystal on the side face of the IC chip 5," there is no clear explanation of the basis for this statement. Because the object of JP 63-117445 is to polish the reverse face only, there is no teaching or suggestion of the need for side face polishing. As such, Applicant believes the smooth cut face referred to in JP 63-117445 results from the dicing process.

At least because of these distinct differences between the method of claim 1 and the method disclosed in JP 63-117445, Applicant submits that JP 63-117445 does not render obvious the subject matter of claim 1 or its dependent claims 3-5, 9, 13 and 14.

Claim 2 was rejected under 35 U.S.C. Section 103(a) as allegedly being obvious over JP 63-117445 in view of the admitted prior art as to testing prior to semi-full dicing. However, testing prior to semi-full dicing does not remedy the above-identified deficiencies of JP 63-117445 with respect to claim 1 (from which claim 2 depends). As such, claim 2 is believed to be allowable.

Claims 8 and 10-19 were rejected under 35 U.S.C. Section 103(a) as allegedly being obvious over JP 63-117445 in view of JP 7-22358. JP 7-22358 discloses a process in which rear-face polishing is performed prior to a semi-full dicing process. JP 7-22358 also discloses that the rear face of a semiconductor wafer is affixed onto a dicing tape through a carrier frame. Here again, however, JP 7-22358 does not remedy the above-identified deficiencies of JP 63-117445 with respect to claim 1 (from which claims 8 and 10-19 depend). As such, claims 8 and 10-19 are believed to be allowable.

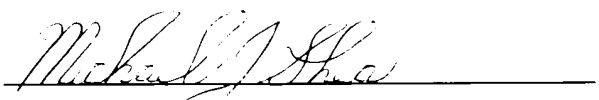
New claims 20-42 are added for the Examiner's consideration. The subject matter of these new claims is fully supported by the original disclosure and no new matter is added. It is respectfully submitted that the applied art does not disclose or suggest the subject matter of these new claims.

Applicants submit that the pending claims are in condition for allowance, and action to that end is earnestly solicited.

If any issues remain to be resolved, the Examiner is urged to contact the attorney for Applicants at the telephone number listed below.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 

Michael J. Shea
Reg. No. 34,725

MJS:led
1100 North Glebe Road, 8th Floor
Arlington, VA 22201-4714
Telephone: (703) 816-4000
Facsimile: (703) 816-4100

Version marked to show changes made

IN THE SPECIFICATION

The paragraph beginning on page 10, line 16 has been amended as follows:

The objective of the present invention is to provide a manufacturing method for a semiconductor device which can carry out a polishing process and a dicing process safely without damaging [giving damages to] the semiconductor wafer, without causing cracks, and without chipping.

The paragraph beginning on page 11, line 22 has been amended as follows:

Therefore, it is possible to eliminate the breaking process after the semi-full dicing process that has been conventionally required, to reduce the number of processes, and also to prevent cracks and chips that used to occur at the time of breaking. Thus, it becomes possible to carry out a polishing process and a dicing process safely without damaging [giving damages to] the semiconductor wafer, without causing cracks and chips.

The paragraph beginning on page 25, line 18 has been amended as follows:

The manufacturing method of a semiconductor device in accordance with the present embodiment is a method in which, after a semi-full dicing process has been carried out from the front face (element formation face) bearing semiconductor elements of a disk-shaped semiconductor wafer, processes such as a rear-face polishing process, a dividing process to each piece of chips and a removing process of a damaged layer (defective areas) such as, a [an]

machining-affected layer and fine cracks, caused by the semi-full dicing process, are simultaneously carried out.

The paragraph beginning on page 30, line 8 has been amended as follows:

In the chemical etching process (S6, Fig. 2(f)), with the front face of the semiconductor wafer 1 (element formation face) being protected by the film 13, a damaged area on a cut face 7a of a semiconductor chip 7 resulting [resulted] from a semi-full dicing process (S3, Fig. 2(c)) is removed by the chemical etching process, and the rear-face polishing process of the semiconductor wafer 1 and the dividing process thereof into individual semiconductor chips 7 are also carried out.

The paragraph beginning on page 30, line 17 has been amended as follows:

In other words, the semiconductor wafer 1, affixed onto the film 13 secured to the carrier frame 14, is immersed into, for example, a hydro-fluoric acid based etchant at a normal temperature of 25°C. Thus, while the front face (element formation face) is being protected by the film 13, the semiconductor wafer 1 is chemically etched so that it becomes possible to simultaneously carry out the rear-face polishing process of the semiconductor wafer 1, the dividing process into individual semiconductor chips 7 and the removing process of a damaged layer, such as a machining-affected layer and cracks, in the cut face 7a of the semiconductor chip 7 due to the semi-full dicing process.

The paragraph beginning on page 31, line 6 has been amended as follows:

In the etchant, first, the semiconductor wafer 1 is etched from the rear face of the semiconductor chip 7 in the thickness direction. In this case, the dicing residual portion is simultaneously etched from the rear face so that when the etching has reached the dicing residual amount of the semi-full dicing process, the semiconductor wafer 1 is separated into semiconductor chips 7. Then, after the separation into the semiconductor chips 7, the etchant enters a groove between the adjacent semiconductor chips 7, with the result that the conductor chip 7 is also etched in the width direction from the cut surface 7a; thus, the damaged layer (defective areas) resulting [resulted] from the semi-full dicing process is also removed. Here, the application of a bonding agent having a chemical etching resistant property in joining the semiconductor wafer 1 to the film 13 makes it possible to prevent the etchant from entering the bonding face of the semiconductor wafer 1 and from etching the front face (element formation face).

The paragraph beginning on page 35, line 23 has been amended as follows:

As described above, even in the case of the application of the device shown in Fig. 5 or Fig. 6, by using the chemical etching process, a damaged layer (defective areas) on the rear face of the semiconductor wafer 3 caused by the polishing process and a damaged layer (defective areas) such as a machining-affected layer and fine cracks in the chip cut face caused by the semi-full dicing process, can be removed while the front face (element formation face) of the semiconductor wafer 3 is being protected, and simultaneously with these processes, the rear-face polishing process of the semiconductor wafer 3 and the separation to individual chips from the

semi-full dicing state through the removal of the dicing residual portion can be carried out at the same time.

The paragraph beginning on page 37, line 20 has been amended as follows:

Moreover, by adopting a carrier system using a carrier frame 14(14'), the chemical etching can be carried out on the basis of each sheet of the semiconductor wafer 1 or on the basis of one lot including a plurality of sheets thereof; therefore, it is advantageous from the viewpoint of mass production [massproduction].

The paragraph beginning on page 38, line 14 has been amended as follows:

Referring to Figs. 7 and 8, the following description will discuss another embodiment of the present invention. Here, for convenient [convenience] explanation, in the present embodiment, those members that have the same functions and that are described in Embodiment 1 are indicated by the same reference numerals and the description thereof is omitted.

The paragraph beginning on page 42, line 10 has been amended as follows:

In the chemical etching process (S14, Fig. 8(d)), with the front face of the semiconductor wafer 1 (element formation face) being protected by the film 16, a damaged area on a cut face 7a of a semiconductor chip 7 resulting [resulted] from a semi-full dicing process (S13, Fig. 8(c)) is removed by the chemical etching process, and the rear-face polishing process of the semiconductor wafer 1 and the dividing process thereof into individual semiconductor chips 7 are also carried out.

The paragraph beginning on page 42, line 19 has been amended as follows:

In other words, the semiconductor wafer 1, affixed onto the film 16 secured to the carrier frame 14', is immersed into, for example, a hydro-fluoric acid based etchant at a normal temperature of 25°C. Thus, while the front face is being protected by the film 16, the semiconductor wafer 1 is chemically etched so that it becomes possible to simultaneously carry out the rear-face polishing process of the semiconductor wafer 1, the dividing process into individual semiconductor chips 7 and the removing process of a damaged layer, such as a machining-affected layer and cracks, in the cut face 7a of the semiconductor chip 7 due to the semi-full dicing process.

The paragraph beginning on page 43, line 7 has been amended as follows:

In the etchant, first, the semiconductor wafer 1 is etched from the rear face thereof in the thickness direction of the semiconductor chip 7. Simultaneously, since the etchant enters [enter] a groove between the adjacent semiconductor chips 7, the dicing residual portion is etched from the rear face so that when the etching has reached the front face (element formation face) of the semiconductor wafer 1 through the dicing residual amount, the semiconductor wafer 1 is separated into semiconductor chips 7. Moreover, at the same time, the semiconductor chip 7 is also etched in the width direction from the cut surface 7a; thus, the damaged layer (defective areas) resulting [resulted] from the semi-full dicing process is also removed. Here, the application of a bonding agent having a chemical etching resistant property in affixing the

semiconductor wafer 1 onto the film 16 makes it possible to prevent the etchant from entering the bonding face of the semiconductor wafer 1 and from etching the front face.

The paragraph beginning on page 44, line 22 has been amended as follows:

Moreover, by adopting a carrier system using the carrier frame 14', the chemical etching can be carried out on the basis of each sheet of the semiconductor wafer 1 or on the basis of one lot including a plurality of sheets thereof; therefore, it is advantageous from the viewpoint of mass production [massproduction].

The paragraph beginning on page 46, line 25 has been amended as follows:

Referring to Figs. 9 and 10, the following description will discuss still another embodiment of the present invention. Here, for convenient [convenience] explanation, in the present embodiment, those members that have the same functions and that are described in Embodiments 1 and 2 are indicated by the same reference numerals and the description thereof is omitted.

The paragraph beginning on page 50, line 8 has been amended as follows:

As described above, with the manufacturing method of a semiconductor device in accordance with the present embodiment, the damaged layer (defective areas), such as a machining-affected layer and fine cracks, on the rear face of a semiconductor wafer resulting [resulted] from the rear-face polishing process can be removed by the chemical etching; thus, it becomes possible to eliminate an unwanted stress exerted on the polished face and deflection in

the semiconductor wafer, which have been conventional problems. Moreover, these effects are particularly advantageous in the manufacturing process of thin-film semiconductor wafers which have difficulties in transporting and handling.

The paragraph beginning on page 50, line 25 has been amended as follows:

The manufacturing method of a semiconductor device of the present invention, which is a semiconductor-wafer polishing and dicing method for dividing the semiconductor wafer into individual devices, may have the steps of: semi-full dicing the semiconductor wafer from the front face (element formation face); forming a protective layer having a chemical etching resistant property on the front face of the semiconductor wafer; removing damaged areas (defective areas), such as a machining-affected layer and fine cracks, on a chip cut face resulting [resulted] from the semi-full dicing process, by using chemical etching while the front face of the semiconductor wafer is being protected, as well as simultaneously carrying out a wafer rear-face polishing process and a removing process of a dicing residual portion from a semi-full dicing state by the chemical etching so that the semiconductor wafer is divided into individual chips; and removing the protective layer having a chemical etching resistant property.

The paragraph beginning on page 52, line 4 has been amended as follows:

Moreover, since the semiconductor wafer can be dealt on the basis of each piece as well as on the basis of one lot, it is superior in the working efficiency at the time of mass production [massproduction], and particularly advantageous in the manufacturing process of thin-film semiconductor wafers which have difficulties in transporting and handling.

The paragraph beginning on page 52, line 18 has been amended as follows:

The manufacturing method of a semiconductor device of the present invention, which is a semiconductor-wafer polishing and dicing method for dividing the semiconductor wafer into individual devices, may have the steps of: forming a protective layer having dicing resistant and chemical etching resistant properties on the front face (element formation face) of the semiconductor wafer; semi-full dicing the semiconductor wafer from the rear face of the semiconductor wafer; removing damaged areas (defective areas), such as a machining-affected layer and fine cracks, on a chip cut face resulting [resulted] from the semi-full dicing process, by using chemical etching while the front face (element formation face) of the semiconductor wafer is being protected, as well as simultaneously carrying out a wafer rear-face polishing process and a removing process of a dicing residual portion from a semi-full dicing state by the chemical etching so that the semiconductor wafer is divided into individual chips; and removing the protective layer having a chemical etching resistant property.

The paragraph beginning on page 53, line 19 has been amended as follows:

The manufacturing method of a semiconductor device of the present invention, which is a semiconductor-wafer polishing and dicing method for dividing the semiconductor wafer into individual devices, may have the steps of: after polishing the semiconductor wafer prior to dicing, semi-full dicing the semiconductor wafer from the front face (element formation face) or the rear face of the semiconductor wafer; forming a protective layer having a chemical etching resistant property on the front face of the semiconductor wafer; removing damaged areas

(defective areas), such as a machining-affected layer and fine cracks, on the rear face of the semiconductor wafer resulting [resulted] from the rear-face polishing process, as well as damaged areas (defective areas) on a chip cut face resulting [resulted] from the semi-full dicing process, by using chemical etching while the front face of the semiconductor wafer being protected, as well as simultaneously carrying out a wafer rear-face polishing process and a removing process of a dicing residual portion from a semi-full dicing state by the chemical etching so that the semiconductor wafer is divided into individual chips; and removing the protective layer having a chemical etching resistant property.

The paragraph beginning on page 56, line 11 has been amended as follows:

In other words, in the chemical etching process, first, the semiconductor wafer is etched from the rear face thereof in the thickness direction of the semiconductor chip. At this time, the dicing residual portion is simultaneously etched from the rear face so that when the etching has reached the thickness of the dicing residual portion (dicing residual amount) left in the semi-full dicing process, the semiconductor wafer is divided into individual semiconductor chips. After the semiconductor chips have been separated, the etchant is allowed to enter a groove between the adjacent semiconductor chips formed in the semi-full dicing process, with the result that the semiconductor chip is etched also in the width direction from its cut face; thus, it is possible to remove damaged areas resulting [resulted] from the semi-full dicing process.

The paragraph beginning on page 60, line 13 has been amended as follows:

Furthermore, the manufacturing method of the semiconductor device in accordance with the present invention may include the rear-face polishing process for polishing the rear face that is the face opposite to the element formation face of the semiconductor wafer, prior to the semi-full dicing process, and may remove the damaged areas on the rear face of the semiconductor wafer resulting [resulted] from the rear-face polishing process during the chemical etching process.

The paragraph beginning on page 60, line 22 has been amended as follows:

The above-mentioned method makes it possible to remove damaged areas such as a machining-affected layer and fine cracks on the rear face of the semiconductor wafer resulting [resulted] from the rear-face polishing process and damaged areas on a chip cut face resulting [resulted] from the semi-full dicing process thereafter through the chemical etching process, while protecting the element formation face. Simultaneously with this process, the rear-face polishing process of the semiconductor wafer is carried out, and the dividing process into individual semiconductor chips from a semi-full dicing state is also carried out by removing the dicing residual portion.

The paragraph beginning on page 62, line 11 has been amended as follows:

Consequently, the chemical etching can be carried out on the basis of each sheet of the semiconductor wafer or on the basis of one lot including a plurality of sheets thereof; therefore, it is advantageous from the viewpoint of mass production [massproduction]. This superior working efficiency at the time of mass production [massproduction] becomes particularly

effective in the manufacturing process of thin-film wafers that have difficulties in transportation and handling.

IN THE CLAIMS

1. (Amended) A manufacturing method for a semiconductor device comprising the steps of:

semi-full dicing a semiconductor wafer so as to leave a dicing residual portion with a predetermined thickness between devices on the semiconductor wafer;

forming a protective layer having a chemical etching resistant property on an element formation face of the semiconductor wafer; and

chemically etching the semiconductor wafer having the protective layer formed on the element formation face from the rear face side so as to polish the rear face of the semiconductor wafer, [so as] to remove the dicing residual portion to divide the semiconductor wafer into individual semiconductor chips, and to remove damaged areas in a cut face of the semiconductor wafer resulting [resulted] from the semi-full dicing process.

2. (Amended) The manufacturing method for a semiconductor device as defined in claim 1, further comprising the step of:

prior to the semi-full dicing step [process], carrying out an electrical test on the semiconductor wafer by means of probing.

3. (Amended) The manufacturing method for a semiconductor device as defined in claim 1, further comprising the step of:

removing the protective layer from the semiconductor chips [that have been individually divided,] after the chemical etching step [process].

4. (Amended) The manufacturing method for a semiconductor device as defined in claim 1, wherein in the semi-full dicing step [process], the semiconductor wafer is subjected to semi-full dicing from the element formation face so as to leave a dicing residual portion with a predetermined thickness on the [side of the] rear face side [that is opposite to the element formation face] of the semiconductor wafer.

5. (Amended) The manufacturing method for a semiconductor device as defined in claim 4, wherein [in the protective layer forming process after the semi-full dicing process,] the protective layer [having a chemical etching resistant property] is formed on the element formation face of the semiconductor wafer.

6. (Amended) The manufacturing method for a semiconductor device as defined in claim 1, wherein in the semi-full dicing step [process], the semiconductor wafer is subjected to semi-full dicing from the [side of the] rear face [that is opposite to the element formation face] so as to leave a dicing residual portion with a predetermined thickness on the element formation face side of the semiconductor wafer.

7. (Amended) The manufacturing method for a semiconductor device as defined in claim 6, wherein [in the protective layer forming process before the semi-full dicing process,] the protective layer [having a dicing protective property and a chemical etching resistant property] is formed on the element formation face of the semiconductor wafer.

8. (Amended) A [The] manufacturing method for a semiconductor device [as defined in claim 1, further] comprising the steps [step] of:

[prior to the semi-full dicing process,] polishing a [the] rear face of a semiconductor wafer that is opposite to an [the] element formation face of the semiconductor wafer;[,]

semi-full dicing the semiconductor wafer so as to leave a dicing residual portion with a predetermined thickness between devices on the semiconductor wafer;

forming a protective layer having a chemical etching resistant property on the element formation face of the semiconductor wafer; and

chemically etching the semiconductor wafer having the protective layer formed on the element formation face from the rear face side so as to remove [wherein in the chemical etching process,] damaged areas on the rear face of the semiconductor wafer resulting [resulted] from the rear-face polishing step [process are removed], to remove the dicing residual portion to divide the semiconductor wafer into individual chips, and to remove damaged areas in a cut face of the semiconductor wafer resulting from the semi-full dicing step.

9. (Amended) The manufacturing method for a semiconductor device as defined in claim 1, wherein the protective layer is a film [having a chemical etching resistant property].

10. (Amended) The manufacturing method for a semiconductor device as defined in claim 1, wherein the protective layer is a chemical etching resistant film of an [a] ultraviolet separation type, which has a reduction in adhesive strength upon irradiation with ultraviolet rays.

11. (Amended) The manufacturing method for a semiconductor device as defined in claim 1, wherein the protective layer is a chemical etching resistant film of a thermal [foaming] type, which has a reduction in adhesive strength upon application of heat.

13. (Amended) The manufacturing method for a semiconductor device as defined in claim 1, further comprising holding [wherein] the protective layer [is held by a protective layer holding means] with a uniform tension during the chemical etching step.

14. (Amended) The manufacturing method for a semiconductor device as defined in claim 13, wherein the uniform tension is maintained on said protective layer by a protective layer holding means [is] placed on a [face] surface of said protective layer that is opposite to the [face] surface of said protective layer on which the semiconductor wafer [with the protective layer] is affixed.

15. (Amended) The manufacturing method for a semiconductor device as defined in claim 13, wherein the uniform tension is maintained on said protective layer by a protective

layer holding means [is] placed on the same surface of said protective layer as [face on which] the semiconductor wafer [with the protective layer is affixed].

16. (Amended) The manufacturing method for a semiconductor device as defined in claim 1, further comprising placing a protective layer holding means having a chemical etching resistant property on [wherein the protective layer has] a peripheral portion of the protective layer [on which a protective layer holding means having a chemical etching resistant property is placed in a manner] so as to surround the entire circumference of the semiconductor wafer.

17. (Amended) The manufacturing method for a semiconductor device as defined in claim 16, wherein the protective layer holding means has a ring shape with a flat bonding face for bonding with the protective layer.

18. (Amended) The manufacturing method for a semiconductor device as defined in claim 17, wherein the protective layer holding means has a draining means for draining etchant remaining inside the protective layer holding means during the chemical etching step [process].

19. (Amended) The manufacturing method for a semiconductor device as defined in claim 18, wherein the draining means is formed [provided] as grooves extending in a radial manner [from the center of the semiconductor wafer].